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APPLICATION FOR LETTERS PATENT

for

RESIDUE-FREE CONTACT OPENINGS AND METHODS FOR FABRICATING SAME

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RESIDUE-FREE CONTACT OPENINGS AND METHODS FOR FABRICATING SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application Serial No. 09/035,497, filed March 5, 1998, pending.

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to fabricating a via employed in an integrated circuit which is substantially free of metal polymer and oxide polymer residues. More particularly, the present invention relates to a two-step via cleaning process which removes metal polymer and oxide polymer residues from a via with substantially no damage to the via or underlying structures carried on a semiconductor substrate.

State of the Art: Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. One commonly used technique in the fabrication of integrated circuits involves stacking of multiple layers of active and passive components one atop another to allow for multilevel electrical interconnection between devices formed on each of these layers. This multilevel electrical interconnection is generally achieved with a plurality of metal-filled vias ("contacts") extending through dielectric layers which separate the component layers from one another. These vias are generally formed by anisotropically etching through each dielectric layer by etching methods known in the industry, such as plasma etching and reactive ion etching. A fluorinated gas, such as CF_4, CHF_3, C_2F_6, CH_2F_2, SF_6, or other freons, and mixtures thereof, in combination with a carrier gas, such as Ar, He, Ne, Kr, O_2, or mixtures thereof, is usually used as the etching gas for these etching methods. A problem with such etching methods is that at least one layer of residue forms in the vias as a result of the etching process.

An exemplary method for forming a via through a dielectric layer is illustrated in FIGs. 11-14. It should be understood that the figures presented in conjunction with this description are not meant to be actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized representations which are employed to more clearly and fully depict the process of this typical method than would otherwise be possible.

FIG. 11 illustrates an intermediate structure 200 comprising a semiconductor substrate bearing a dielectric or insulating layer 202 (such as an oxide) having a metal-containing trace or pad 204 of aluminum, aluminum alloys, titanium, titanium/tungsten alloys, molybdenum, or the like, formed thereon. The term "semiconductor substrate" is used herein to denote any solid semiconductor surface, such as is provided by a silicon or gallium arsenide wafer, or a layer of such material formed on glass, ceramic, sapphire, or other supporting carrier, as known in the art, and includes such semiconductor surfaces bearing an insulating layer thereon. A barrier layer 206 (such as titanium nitride) extends over the metal-containing trace or pad 204, and an interlayer dielectric 208 (such as silicon dioxide) is disposed over the barrier layer 206. As shown in FIG. 12, the interlayer dielectric 208 is masked with a resist material 212, which is then patterned to define a via location. A partial via 214 is then selectively etched with a fluorinated gas down to the barrier layer 206, which acts as an etch stop. The etching of the partial via 214 results in a first residue layer 216 of a carbon-fluorine based, polymer-containing residue of the interlayer dielectric 208 ("oxide polymer") coating the sidewall 218 of the partial via 214, as shown in FIG. 13. The barrier layer 206 at the bottom of partial via 214 is then etched to expose the metal-containing trace or pad 204 and form a full via 222, as shown in FIG. 14. However, due to the variation in the thickness of the interlayer dielectric 208 from the center of the wafer to the edge (usually between 4000 and 5000Å), an oxide over-etch is applied, such that the via will usually extend through the barrier layer 206 and into the metal-containing trace or pad 204. When the barrier layer 206 and metal containing trace or pad 204 are etched, a second residue layer 224 ("metal polymer") of a carbon-fluorine

based polymer including metal etched from the metal-containing trace or pad 204, as well as any metal components in the barrier layer 206, such as the titanium in a titanium nitride barrier layer, is formed over the first residue layer 216 and the exposed surface 226 of the metal-containing trace or pad 204, also shown in FIG. 14. It is, of course, understood that a single etch could be performed to expose the metal-containing trace or pad 204, which etch would result in a single residue layer. However, even if a single etch were performed, the single residue layer would still have a portion of the residue layer adjacent the via sidewall 218 containing primarily oxide polymer and a portion adjacent the via aperture and the bottom of the via containing primarily metal polymer.

Residue layers, such as first residue layer 216 and second residue layer 224, which coat the full via, are very difficult to remove. These residue layers may be removed by dipping the structure in a 35°C phosphoric acid solution, preferably about a 20:1 ratio (volume of water to volume of acid) solution, for about 90 seconds. Although this technique is effective in removing most of the residue layers, the residue layers are still not completely removed. The portion of the residue still remaining after the phosphoric acid dip adversely affects the conductivity of contacts subsequently formed in the full via 222. It is noted, that although extending the residence time of the semiconductor substrate structure in the phosphoric acid will effectively remove all of the residue layer(s), the increased residence time also results in damage to the metal-containing trace or pad 204.

Thus, it can be appreciated that it would be advantageous to develop a technique to clean substantially all of the residue layer(s) from a semiconductor via without substantial damage to the metal-containing trace or pad while using commercially-available, widely-practiced semiconductor device fabrication techniques.

BRIEF SUMMARY OF THE INVENTION

The present invention relates to a two-step via cleaning process which removes metal polymer and oxide polymer residues from a via in a dielectric layer with

substantially no damage to the via or underlying structures. One embodiment of the present invention relates to the removal of the metal polymer and oxide polymer residues after the formation of the via. The via is formed through a dielectric layer and a barrier layer which are disposed over a metal-containing trace, pad, or other circuit element, wherein the metal-containing trace, pad, or other circuit element is disposed on a semiconductor substrate over the aforementioned oxide or other insulator. When such a via is formed, the sidewall of the via is coated with a residue layer. The residue layer generally has two distinct components: an oxide polymer layer and a metal polymer layer.

The two-step cleaning process of the present invention completely removes both components of the residue layer. The residue layer is first subjected to a nitric acid dip to remove the metal polymer layer and expose the oxide polymer layer. The oxide polymer layer is then subjected to a phosphoric acid solution dip to remove the oxide polymer layer. It has also been found that fluorine containing mixtures, such as hydrofluoric acid (HF) and ammonium fluoride (NH_4F), may be used in lieu of the phosphoric acid solution or mixed with phosphoric acid for removal of the oxide polymer layer.

The oxide polymer and metal polymer layers may also be removed during the fabrication of the via, between the formation of the partial via and its extension to the underlying trace and after the full via formation, respectively. A partial via, or first via portion, is formed by masking the dielectric layer and etching through to the barrier layer (etch stop) which forms the oxide polymer residue on the walls of the partial via. The oxide polymer residue is then subjected to a phosphoric acid solution dip, which removes the oxide polymer residue. The barrier layer is then etched to extend the via in a second via portion to expose the metal-containing trace and form a full via. When the barrier layer is etched, the metal polymer layer is formed. The metal polymer layer is then subjected to a nitric acid dip which removes the metal polymer layer. Once a clean full via is achieved, a contact may be completed by, as known in the art, depositing a conductive material into the via.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1-3 are side cross-sectional views of a method of removing residue material from a via according to a technique of the present invention;

FIGS. 4-9 are side cross-sectional views of a method of removing residue material while forming a via according to another technique of the present invention;

FIG. 10 is a side cross-sectional view of a contact formed according to a technique of the present invention; and

FIGS. 11-14 are side cross-sectional views of a via formation process according to a known technique.

DETAILED DESCRIPTION OF THE INVENTION

FIGs. 1-3 illustrate one embodiment according to the present invention for removing residue layers from a via. It should be understood that the figures presented in conjunction with this description are not meant to be actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized representations which are employed to more clearly and fully depict the process of the invention than would otherwise be possible.

FIG. 1 illustrates a via 106 in an intermediate structure 100 in the production of a semiconductor device (similar to FIG. 14) directly after the etching of the via 106. This intermediate structure 100 comprises a semiconductor substrate bearing an exposed insulating or dielectric layer 102, such as an oxide, having a metal-containing trace or pad 104 of aluminum, aluminum alloys, titanium, titanium/tungsten alloys, molybdenum, or the like, disposed thereon. The via 106 extends through a dielectric layer 108, such as silicon dioxide or the like, and a barrier layer 112, such as silicon nitride, which are disposed over the oxide insulator 102. The sidewalls 114 of the

via 106 are coated with a residue layer 116. As used herein, the term "sidewall" of a via encompasses both a single, continuous sidewall, such as may define a round or circular via, as well as a plurality of sidewalls defining a via of another cross-section.

The presence of the residue layer 116 is a natural consequence of the etching of the via 106 and generally comprises two distinct layers: an oxide polymer layer 118 and a metal polymer layer 120. As previously discussed, a partial via or first via portion may be selectively etched through an etch mask 122 down through the dielectric layer 108 to the barrier layer 112 (an etch stop) which results in the oxide polymer layer 118, which is usually a carbon-fluorine based, polymer-containing residue of the dielectric layer 108, coating the sidewalls of the partial via. The barrier layer 112 may be then etched to create a second, contiguous via portion and expose the metal-containing trace or pad 104, thereby forming the via 106.

As discussed above, due to thickness variations in the dielectric layer 108, the barrier layer 112 is typically over-etched such that the etch will usually extend through the barrier layer 112 and into the metal-containing trace or pad 104. When the barrier layer 112 and underlying metal-containing trace or pad 104 are etched, a metal polymer layer 120 is formed atop the oxide polymer layer 118. The metal polymer layer 120 usually comprises a carbon-fluorine based polymer including metal etched from the metal-containing trace or pad 104, as well as any metal components in the barrier layer 112, such as the titanium in a titanium nitride barrier layer 112. Again, as previously discussed, a single etch could be performed to penetrate dielectric layer 108 and barrer layer 112 and expose the metal-containing trace or pad 104 which would result in a single residue layer. However, the single residue layer would still have an inner portion of the residue layer adjacent the via sidewall 114 containing primarily an oxide polymer and a outer portion adjacent the via 106 containing primarily a metal polymer.

It has been found by the inventors that a concentrated nitric acid is effective in removing the metal polymer layer 120 portion of the residue layer 116, and phosphoric acid is effective in removing the oxide polymer layer 118 portion of the residue layer

116. However, it has been found by the inventors that it was not possible to completely remove all of the residue layer 116 by either phosphoric acid application or nitric acid application alone. It was further found by the inventors that attempts to completely remove the residue layer 116 by increasing the residence time in the phosphoric acid results in damage to the barrier layer 112 and/or the metal-containing trace or pad 104. Furthermore, mixtures of phosphoric acid and nitric acid were also found to be unacceptable for removal of the residue layer 116.

Thus, a two-step cleaning process may be used to substantially remove the entire residue layer 116. The residue layer 116 is first subjected to a nitric acid dip for about 200 seconds to remove the metal polymer layer 120 and expose the oxide polymer layer 118, as shown in FIG. 2. The nitric acid dip may preferably contain between about 50% and 100% by weight nitric acid, most preferably about 70% by weight, and preferably at a temperature between about 10°C and 100°C, most preferably about 25°C. The duration of the nitric acid dip is preferably between about 10 seconds and 30 minutes, most preferably 200 seconds. However, the duration of the nitric acid dip will depend on the concentration and temperature of the nitric acid dip.

The oxide polymer layer 118 is then subjected to a 35°C phosphoric acid solution dip, preferably about a 20:1 ratio (volume of water to volume of acid) solution, for about 90 seconds, which removes the oxide polymer layer 118, as shown in FIG. 3, after the etch mask 122 has been removed. The phosphoric acid solution dip may be in a concentration between about 200:1 and 1:1 volumetric ratio of water to acid at a temperature of between about 10° and 80°C. The duration of the phosphoric acid solution dip is preferably between about 10 seconds and 10 minutes. However, the duration of the phosphoric acid dip will depend on the concentration and temperature of the dip.

In an experiment employing the aforementioned, nitric acid and phosphoric acid dips were used to clean vias of depths ranging from 0.4 to 0.7 microns and having diameters ranging from 0.4 to 1 micron and exhibiting metal polymer layers of

approximately 200Å in thickness and oxide polymer layers of approximately 300Å in thickness. A nitric acid dip was used at about 70% by weight nitric acid, at about ambient room temperature and for a duration of about 200 seconds. A subsequent phosphoric acid dip at about a 20:1 ratio acid to water volume was employed at about 35°C for about 90 seconds. No detectable metal polymer or oxide polymer remained in the vias after treatment. Thus, a nitric acid dip of about 100 seconds was demonstrated to remove about 100Å in thickness of oxide polymer.

It has also been found that the oxide polymer layer 118 can be removed by subjecting the oxide polymer layer 118 to a dip in fluorine containing mixtures; for example, components such as hydrofluoric acid (HF) and ammonium fluoride (NH_4F) may be used in lieu of the phosphoric acid solution or mixed with phosphoric acid for removal of the oxide polymer layer. A preferred concentration for such fluorine-containing mixtures may range from about 0.01% to about 2%.

As illustrated in FIGs. 4-9, the two-step process may also be effected during the formation of a via. Elements common between FIGs. 1-3 and 4-9 retain the same numeric designation. FIG. 4 illustrates an intermediate structure 150 comprising a semiconductor substrate bearing an oxide insulator 102 having a metal-containing trace or pad 104 formed thereon. A barrier layer 112, such as silicon nitride, extends over the metal-containing trace or pad 104 and an dielectric layer 108, such as silicon dioxide, is disposed over the barrier layer 112. As shown in FIG. 5, the dielectric layer 108 is masked with an etch mask 122, which is patterned to define the via location. A partial via or first via portion 152 is then selectively etched down to the barrier layer 112 (an etch stop) which results in the oxide polymer layer 118, which is usually a carbon-fluorine based, polymer-containing residue of the dielectric layer 108, coating the sidewalls of the partial via 152, as shown in FIG. 6. The oxide polymer layer 118 is then subjected to a phosphoric acid solution dip, preferably about a 20:1 volume ratio of water to phosphoric acid at about 35°C for about 90 seconds, to remove the oxide polymer layer 118, as shown in FIG. 7.

The barrier layer 112 is then etched to form a second via portion and expose the metal-containing trace or pad 104, thereby forming a full via 156, as shown in FIG. 8. When the barrier layer 112 is etched, as discussed above, a metal polymer layer 120 is formed which is usually a carbon-fluorine based polymer including metal etched from the metal-containing trace or pad 104, as well as any metal components in the barrier layer 112. The metal polymer layer 120 is then subjected to a nitric acid dip, preferably approximately 70% volume nitric acid for about 200 seconds, which removes the metal polymer layer 120, as shown in FIG. 9, after the etch mask 122 has been removed.

Once a clean via is achieved, a contact 160 may be completed by depositing a conductive material 162 into the via, as shown in FIG. 10. The conductive material 162 is preferably a metal, including but not limited to copper, silver, gold, aluminum (preferred), and alloys thereof. However, conductive polymers may be used. The deposition of the conductive material 162 may be effected by methods including, but not limited to, hot sputter/reflow, ionized plasma, hot pressure fill, as well as physical vapor deposition and chemical vapor deposition combinations.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.